In the Claims:

1. (Previously Presented) A phase change memory cell fabricated by integrated circuit techniques on a semiconductor substrate, comprising:

an insulating, dielectric layer on the substrate;

a thin conductive film having a first film thickness on the dielectric layer, the plane of the film being generally parallel to the plane of the substrate;

a layer of a phase change material having a second film thickness supported by the dielectric layer; and

an electrically resistive interface between the thin conductive film and the phase change material layer, the interface being defined by an area of engagement between the film and the layer that is generally normal to the plane of the substrate, and wherein the thickness of the thin conductive film is less than the thickness of the layer of phase change material at the interface.

2. (Original) The memory cell of Claim 1, wherein:

the electrical resistance of the interface is inversely proportional to the area of engagement; and

the width of the conductive film generally parallel to the plane of the substrate and the height of the conductive film generally normal to the plane of the substrate determine the area of engagement.

3. (Original) The memory cell of Claim 2, wherein the width of the conductive film generally parallel to the plane of the substrate is determined by photolithography and the height of the conductive film generally normal to the plane of the substrate is determined by deposition parameters.

4. (Original) The memory cell of Claim 3, wherein heat produced by current through the interface flows from the interface into the phase change material layer in a direction generally parallel to the plane of the substrate.

5. (Original) The memory cell of Claim 4, which further comprises a contact on the phase change material layer, wherein:

a current path from the interface into the phase change material layer lies in a direction substantially parallel to the plane of the substrate; and

a current path from the phase change material layer into the contact lies in a direction generally normal to the plane of the substrate.

6. (Original) The memory cell of Claim 1, wherein the phase change material layer and the thin conductive film are not relatively superjacent or subjacent.

7. (Original) The memory cell of Claim 6, wherein the phase change material layer resides in a trench formed in the dielectric layer, the bottom surface of the trench and the phase change material layer being coplanar with or below the lower surface of the dielectric layer.

8. (Original) The memory cell of Claim 7, further comprising a transistor formed in and on the substrate and in the dielectric layer, and wherein an output of the transistor is electrically continuous with one terminus of the thin conductive film, the other terminus of the thin conductive film engaging the dielectric layer to define the interface.

9. (Previously Presented) A phase change memory cell fabricated by integrated circuit techniques on a semiconductor substrate, comprising:

an insulating, dielectric layer on the substrate;

a thin conductive film on the dielectric layer, the plane of the film being generally parallel to the plane of the substrate;

a layer of a phase change material supported by the dielectric layer, wherein the phase change material layer and the thin conductive film are not relatively superjacent or subjacent and wherein the phase change material layer resides in a trench formed in the dielectric layer, the bottom surface of the trench and the phase change material layer being coplanar with or below the lower surface of the dielectric layer;

an electrically resistive interface between the thin conductive film and the phase change material layer, the interface being defined by an area of engagement between the film and the layer that is generally normal to the plane of the substrate; and

a transistor formed in and on the substrate and in the dielectric layer, and wherein an output of the transistor is electrically continuous with one terminus of the thin conductive film, the other terminus of the thin conductive film engaging the dielectric layer to define the interface, wherein the thin conductive film is generally coplanar with a gate electrode of the gate.

10. (Original) The memory cell of Claim 9, wherein:

the dielectric layer comprises a first, lower stratum, a second intermediate stratum on the first stratum and a third, upper stratum on the second stratum;

the gate electrode and the conductive layer reside on the first stratum, in the second stratum and under the third stratum; and

the phase change material layer resides on the first stratum and in the second and third strata.

11. (Original) The memory cell of Claim 10, further comprising:

a contact on the gate electrode; and

a topmost stratum on the third stratum, wherein the contact on the phase change material layer and the contact on the gate electrode reside in the topmost stratum.

12 – 28 (Canceled).

29. (Previously Presented) An improved phase change memory cell fabricated by integrated circuit techniques on a substrate, the memory cell being of the type in which there is an interface between a layer of phase change material and a conductive element, the area of the interface determining the resistance thereof to current flow therethrough, wherein the improvement comprises:

the conductive element being a thin film of a conductive material that does not overlap, and extends away from, the phase change material layer in a direction generally parallel to the plane of the substrate, the resistance of the interface being determined by the thickness of the

thin film normal to the substrate, and wherein the thickness of the thin film is less than the thickness of the phase change material layer at the interface.

30. (Original) The memory cell of Claim 29, wherein the interface is defined by the engagement of a side of the phase change material layer and an end of the thin film, the side and the end being generally normal to the plane of the substrate.

31. (Original) The memory cell of Claim 29, wherein the conductive material comprises a high bandgap and high thermal conductivity material.

32. (Original) The memory cell of Claim 29, wherein heat produced by current through the interface flows from the interface into the phase change material layer in a direction generally parallel to the plane of the substrate.

33. (Original) The memory cell of Claim 29, the cell further being of the type in which current flows through the phase change layer from the interface to a contact on the phase change material layer, wherein:

current flows from the interface into the phase change material layer in a direction substantially parallel to the plane of the substrate; and

current flows from the phase change material layer into the contact in a direction generally normal to the plane of the substrate.

34. (Original) The memory cell of Claim 29, wherein:

the thin film resides on a dielectric stratum on the substrate; and

the phase change material layer resides in a trench formed in the stratum, the trench defining the length of the thin film toward the phase change material layer in a direction generally parallel to the plane of the substrate.

35. (Original) The memory cell of Claim 29, wherein the width of the thin film generally parallel to the plane of the substrate at the interface is determined by photolithography and the height of the thin film generally normal to the plane of the substrate at the interface is determined by thin film deposition parameters.

36. (Currently Amended) A memory cell, comprising:

a layer of phase change material; and

an elongated thin conductive film having one end engaging a side of the layer to define an interface having a width and a height, at least one dimension of the interface being determined non-photolithographically by thin film deposition parameters[[.]], wherein the thin conductive film and the layer of phase change material engage at an interface and wherein the thin conductive film has a thickness at the interface that is thinner than the phase change material at the interface.

37. (Original) A method of using the memory cell of Claim 36, which comprises applying a voltage across the other end of the film and the layer so that current flows from the interface into the layer generally parallel to the film.

38. (Original) The method of Claim 37, wherein the current flows out of the layer generally normal to the film.